REMARKS

This is intended as a full and complete response to the Office Action dated February 3, 2005, having a shortened statutory period for response set to expire on May 3, 2005. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-22 are pending in the application. Claims 11 and 14-22 remain pending following entry of this response. Claims 1-10 have been canceled without prejudice in response to the restriction requirement. Claims 11, 16 and 19 have been amended. Claims 12-13 have been cancelled. New claims 23-24 have been added to recite aspects of the invention. Claim 16 is objected to because of informalities. Claim 16 has been amended to correct a minor editorial error. Applicants submit that the amendments and new claims do not introduce new matter.

Claim Rejections - 35 USC § 102

Claims 11-15, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by *Lu* (6,218,693). Applicants respectfully traverse this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, *Lu* does not disclose "each and every element as set forth in the claim". For example, *Lu* does not disclose a doped region formed in the source/drain electrode to contact the filling of the bit-line contact, wherein the doped region comprises a locally limited electrically conductive contact layer which is formed underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact. The Examiner argues that *Lu* discloses a memory cell having a doped region as claimed. However, the passages and Figures cited by the Examiner are in fact directed to a

doped conductive layer (reference numeral 19 (N+)) projecting from the source-drain-diffusion region (reference numeral 17 (N-)) in which the conductive layer projects underneath the insulating layer (reference numeral 20) adjoining the bit line contact (reference numeral 30'). *See* Figures 1, 2 and 12 of *Lu*. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Claim Rejections - 35 USC § 103

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Lu* as applied to claims 11-15, 17 and 18 above, and further in view of *Dennison et al.* (6,429,069, hereinafter *Dennison*). The Examiner takes the position that:

> "It would have been within the scope of one of ordinary skill in the art to combine the teachings of *Lu* and *Dennison et al.* to enable the peripheral contacts formation step of *Dennison et al.* to be performed in the process of *Lu* because by making the peripheral contacts and the bit-line contact on the same structure plane and of the similar material, all of them can be made in a single step saving process steps, time and manufacturing costs."

Applicants respectfully traverse this rejection. The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the third criteria.

As discussed above, *Lu* does not disclose "each and every element as set forth in the claim". *Dennison* discloses a method for fabricating a memory cell utilizing self-aligned contact openings. The references cited by the Examiner, either alone or in combination, fail to teach, show or suggest a doped region formed in the source/drain electrode to contact the filling of the bit-line contact, wherein the doped region comprises a locally limited electrically conductive contact layer which is formed underneath the bit-line contact in the diffusion region and which has a relatively reduced

lateral migration underneath the insulator layer adjoining the bit-line contact. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Lu* as applied to claims 11-15, 17 and 18 above, and further in view of *Bollinger et al.* (6,762,136, hereinafter *Bollinger*). The Examiner takes the position that:

> "It would have been within the scope of one of ordinary skill in the art to combine the teachings of *Lu* and *Bollinger et al.* to enable the annealed region formation step of Bollinger et al. to be performed in the process of *Lu* because the annealing will repair the crystal damage done by the implant process in the bit-line contact".

Applicants respectfully traverse this rejection. The present rejection fails to establish that the prior art reference (or references when combined) teach or suggest all the claim limitations. As discussed above, *Lu* does not disclose "each and every element as set forth in the claim". *Bollinger* discloses a rapid thermal processing of substrates. The references cited by the Examiner, either alone or in combination, fail to teach, show or suggest a doped region formed in the source/drain electrode between the substrate and the filling of the bit-line contact, wherein the doped region comprises a locally limited electrically conductive contact layer which is formed underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, Applicants believe that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

Gero G. McClellan
Registration No. 44,227
MOSER, PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicants